REMARKS

The Final Office Action mailed May 13, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Counsel for Applicants respectfully requests an interview with the Examiner to answer any questions the Examiner may have concerning the following remarks and to further discuss the present application in relation to the cited references.

A "Petition for Extension of Time" for extending the due date for responding to the Office Action by one month and a credit card payment form to cover the fee payment ($120.00) for the extension are filed with this Amendment. Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 108066-00030**, for any additional fees necessary for entry of this Amendment.

Claims 1, 6 and 11 have been amended. Applicants submit that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1-17 are pending in the present application and are respectfully submitted for reconsideration.

Claims 1-3, 5-8, 10-13 and 15-17 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yishay et al. patent (U.S. Patent No. 5,704,039) in view of the Akiyama et al. patent (U.S. Patent No. 5,784,464). Dependent claims 2-3 and 5, dependent claims 7-8 and 10, and dependent claims 12-13 and 15-16 depend from independent claims 1, 6 and 11, respectively. Claims 1, 6 and 11 have been amended. The rejections are respectfully traversed and reconsideration is requested.

Independent claim 1, as amended, recites an IC comprising an internal circuit; a debug I/F circuit for debugging the internal circuit externally; and an authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and the transmission key to enable operation of the debug I/F circuit, wherein the internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus, wherein the CPU writes the transmission key to the authentication circuit to start the authentication circuit. Independent claim 6, as amended, recites an electronic device mounted with an IC, as claimed in claim 1. Independent claims 11 and 17, as amended, respectively recite a debugging method and a debugger for debugging an IC, as claimed in claim 1. It is respectfully submitted that neither the Yishay et al. patent nor the Akiyama et al. patent, either alone or in alleged combination, discloses or suggests the IC, the electronic device mounted with an IC, the debugging method and the debugger for debugging an IC, as claimed in the present invention.

In the Office Action, the Examiner took the position that the Yishay et al. patent, with reference to Fig. 1, discloses a circuit that includes a CPU 12 connected to a debug interface circuit through a debug bus (namely, CPU security buffer 13 and bus 24) and a peripheral circuit 14, 16, 18, 20 connected to the CPU through an internal bus separated from the debug bus 36, as recited in the present invention. However, the integrated circuit terminals/pins 24 (referred to as "bus" by the Examiner in the Office Action) and the bus 36 disclosed in the Yishay et al. patent are each neither equivalent nor analogous to the debug bus of the present invention.

Specifically, the Yishay et al. patent merely discloses that information is transferred between each of the components of data processing system 10 via bus 36 using a plurality of integrated circuit terminals 24, 25, 28, 30, 32, 34 and 35. More specifically, the Yishay et al. patent discloses that CPU security buffer 13 is optionally coupled to a device external to data processing system 10 by way of memory security buffer 24 (Fig. 1; col. 6, ls. 46-49; col. 7, ls. 59-65).

In addition, the Yishay et al. patent appears directed to a security feature for the internal memory of a data processor and a circuit for disabling the security feature in which the security mode is accomplished, in part, disabling a background debug mode of operation or another debug mode of operation of the data processor. Indeed, the reference particularly stresses that any debug interface which directly accesses the CPU must be disabled and that the security mode of the data processor is disabled for testing purposes, debugging purposes, and other authorized access. (col. 3, ls. 43-62; col. 4, ls. 16-22 and 28-30) More specifically, when security mode is enabled and data processing system 10 is operating in a background debug mode of operation in which data is transferred between the plurality of integrated circuit pins 24 and CPU 12 and between the plurality of integrated circuit pins 28 and system integration circuit 16, the data values transferred between CPU 12 and the plurality of integrated circuit pins 24 is blocked by CPU security buffer 13 and the data values transferred between the plurality of integrated circuit pins 28 and system integration circuit 16 are also blocked by external bus circuit 156. When the security mode of operation is disabled, communication between an external device and CPU 12 via the plurality of integrated circuit pins 24 and CPU security buffer 13 is restored. (col. 9, ls. 1-11 and 50-54)

In contrast, the present invention discloses an IC, an electronic device, a debug method and a debugger, having a security function for preventing the exploitation of a debug I/F circuit, comprising in part an authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and the transmission key to enable operation of the debug I/F circuit, wherein an internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus, and wherein the CPU writes the transmission key to the authentication circuit to start the authentication circuit.

Furthermore, the Akiyama et al. patent appears to merely disclose a client-server based authentication system in which keys are generated, encrypted and exchanged to verify the identity of a client seeking access to services. Such does not disclose or suggest the IC, the electronic device, the debug method and the debugger of the present invention. Indeed, it does not appear that debug methods, debug I/F circuits and the like are mentioned anywhere in the Akiyama et al. patent. Accordingly, both the Yishay et al. patent and the Akiyama et al. patent fail to disclose the present invention as claimed.

While the Examiner has argued that one cannot show nonobviousness by attacking the references individually where the rejections are based on the combination of the references, when the references are viewed together one cannot import into the combination of references what not is disclosed or suggested by the references viewed together. Accordingly since neither the Yishay et al. patent nor the Akiyama et al. patent discloses or suggests the IC, the electronic device mounted with the IC, the debugging method and the debugger, as claimed in the present invention, it is submitted that the alleged combination of these references also does not disclose

or suggest the present invention as claimed. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention. Specifically, neither the Yishay et al. patent nor the Akiyama et al. patent discloses or suggests preventing the exploitation of a debug I/F circuit during debug mode. Rather, the Yishay et al. patent addresses security by disabling debug mode altogether and the Akiyama et al. patent makes no reference to security when debug mode is enabled. It is therefore submitted that the references, either alone or in alleged combination, fail to disclose or suggest the present invention as claimed. Based upon the forgoing, it is respectfully submitted that independent claims 1, 6, 11 and 17 are patentable and in condition for allowance. Reconsideration is respectfully requested.

It is further submitted that dependent claims 2-3 and 5, dependent claims 7-8 and 10, and dependent claims 12-13 and 15-16 are also patentable and in condition for allowance due to their dependency upon independent claims 1, 6 and 11, respectively, since the dependent claims differ in scope from the corresponding parent claims. Dependent claims 2-3 and 5 depend from independent claim 1, dependent claims 7-8 and 10 depend from independent claim 6 and dependent claims 12-13 and 15-16 depend from independent claim 11, and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims are patentable over the alleged combination of the Yishay et al. patent and the Akiyama et al. patent for at least the reasons set forth above with respect to independent claims 1, 6 and 11.

Dependent claims 4, 9 and 14 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yishay et al. patent in view of the Akiyama et al. patent and further in view of the Matsumura et al. patent (U.S. Patent No. 4,908,038). Dependent claims 4, 9 and 14

depend from independent claims 1, 6 and 11, respectively. The rejections are respectfully traversed and reconsideration is requested.

With reference to the above arguments concerning the independent claims, it is further submitted that the Yishay et al. patent, the Akiyama et al. patent and the Matsumura et al. patent, either each alone or in the alleged combination suggested by the Examiner in the Office Action, do not disclose or suggest the content of dependent claims 4, 9 and 14. As acknowledged by the Examiner, "neither the Yishay et al. patent nor the Akiyama et al. patent teach waiting a specified amount of time before enabling the operation of the debug interface." As argued above, nor do the Yishay et al. patent and the Akiyama et al. patent disclose the IC, the electronic device, the debug method and the debugger of the present invention, having a security function for preventing the exploitation of a debug I/F circuit, comprising in part an authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and the transmission key to enable operation of the debug I/F circuit, wherein an internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus, and wherein the CPU writes the transmission key to the authentication circuit to start the authentication circuit. While the Matsumura et al. patent appears to disclose an IC card security feature in which output of processing result is waited by a timer in order to make a processing time constant from receipt of the processing request to output of the processing result, such also does not disclose or suggest the IC, the electronic device, the debug method and the debugger of the present invention as claimed.

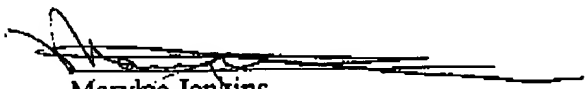
Moreover, there is no suggestion to combine the references, as suggested by the Examiner in the Office Action. Specifically, none of the cited references are directed to preventing the exploitation of a debug I/F circuit when debug mode is enabled. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention since all of the references lack this claimed feature. It is therefore submitted that the dependent claims are also patentable and in condition for allowance. Reconsideration is requested

Entry of this Amendment after final rejection is therefore submitted as proper in that it places the application in condition for allowance. Particularly, the present Amendment is submitted as not raising new issues or requiring further consideration or searching. Undersigned counsel would accordingly appreciate the Examiner telephoning counsel prior to the expiration of the six-month statutory period (i.e., November 13, 2005) to indicate the disposition of this Response.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned counsel at the telephone number, indicated below.

Dated: September 13, 2005

Respectfully submitted,



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